II. AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method for testing an integrated circuit (10) having wells (14, 18) that are wired separately from circuit VDD and ground, the method comprising the steps of:

testing a circuit including independently modifying a p-well (14) bias of an n-transistor (16) and an n-well bias (18) of a p-transistor (20);

storing a result of the testing in a control unit; and

determining whether a defect exists from the stored result of the testing,

wherein the wells (14, 18) include partitions, the modifying step includes applying a different well bias condition to at least one partition compared to at least one other partition, and the determining step is applied to one of the circuit as a whole and on a partition-by-partition basis.

2-3. (Canceled).

4. (Original) The method of claim 1, wherein the testing step further includes stimulating the circuit with a test vector followed by the step of modifying the well biases for a predetermined time prior to the determining step.

5-9. (Canceled).

10. (Original) The method of claim 1, wherein the testing step further includes voltage-based testing.

11. (Canceled).

12. (Currently Amended) The method of claim 10, wherein the voltage-based testing includes applying a low-VDD to the integrated circuit.

13. (Original) The method of claim 10, wherein the modifying step includes:

first setting each well bias at a nominal value;

second increasing the p-well (14) bias of the n-transistor (16) from a nominal value and setting the n-well (18) bias of the p-transistor (20) at a nominal value; and

third setting the p-well bias of the n-transistor at a nominal value and decreasing the n-well bias of the p-transistor from a nominal value,

wherein the determining step occurs between each of the above steps.

14. (Original) The method of claim 13, wherein the modifying step further includes:

fourth setting the p-well (14) bias of the n-transistor (16) to a lower than nominal value and the n-well (18) bias of the p-transistor (20) to a higher than nominal value;

fifth setting the p-well bias of the n-transistor to a lower than nominal value and the n-well bias of the p-transistor to a lower than nominal value;

sixth setting the p-well bias of the n-transistor to a higher than nominal value and the n-well bias of the p-transistor to a higher than nominal value,

wherein the determining step occurs between each of the above steps.

15-31. (Canceled).

32. (Previously Presented) A system for testing a semiconductor circuit (10) having wells (14, 18) that are wired separately from circuit VDD and ground, the system comprising:

means for testing (60) the circuit including independently modifying a well bias of an n-transistor (16) and a well bias of a p-transistor (20);

means for storing a result of the testing in a control unit; and

means for determining (62) whether a defect exists from the stored result of the testing,

wherein the wells (14, 18) include partitions, the well bias modifying includes applying a different well bias condition to at least one partition compared to at least one other partition, and the determining is applied to one of the circuit as a whole and on a partition-by-partition basis.

33. (Original) The system of claim 32, further comprising a temperature sensor (50, 52) for monitoring a temperature of the IC, wherein the means for testing (60) modifies the well biases to maintain a stress test temperature.